**TSMC Technology Scaling Reference Tool - User Guide**

**Overview**

The TSMC Technology Scaling Reference Tool is designed to help VLSI designers, architects, and engineers make informed decisions about technology node migration and early-stage design planning. This tool provides verified scaling data for TSMC processes from 180nm to 2nm, helping you understand the trade-offs between different technology nodes.

**Key Use Cases**

**1. Technology Migration Planning**

* **Scenario**: You have a design on N7 and want to evaluate moving to N5 or N3
* **How to use**: Set N7 as your base node in scaling mode and compare density, power, and performance improvements
* **What to look for**: Area reduction potential, power savings, and cost implications

**2. Early Design Budgeting**

* **Scenario**: Planning a new SoC and need to estimate die area requirements
* **How to use**: Use absolute values mode to see transistor densities across nodes
* **What to look for**: Realistic density numbers for your target applications (remember HP vs HD libraries)

**3. Competitive Analysis**

* **Scenario**: Comparing your technology choices against competitors
* **How to use**: Reference historical data to understand when competitors likely used specific nodes
* **What to look for**: Performance/power/area trade-offs that explain product positioning

**Tool Interface Guide**

**View Modes**

**Absolute Values Mode**

* Shows actual specifications for each technology node
* **Best for**: Understanding real-world parameters and historical trends
* **Key metrics**: Transistor density (MTr/mm²), supply voltage (V), gate length (nm)

**Scaling Factors Mode**

* Shows relative scaling compared to a selected base node
* **Best for**: Migration planning and "what-if" analysis
* **How to read**:
  + > 1.0 = Better than base node
  + = 1.0 = Same as base node
  + < 1.0 = Worse than base node

**Data Table Mode**

* Complete specification table for reference
* **Best for**: Detailed comparisons and documentation
* **Use case**: Including in design reviews or technology selection reports

**Parameter Selection**

**Key Parameters Explained:**

* **Transistor Density**: Logic transistor density in millions of transistors per mm²
  + *Critical insight*: These are high-density (HD) library numbers; actual designs using high-performance (HP) libraries achieve ~30% lower density
* **Gate Delay**: Relative performance metric (lower = faster)
  + *Note*: Actual performance depends heavily on design and operating conditions
* **Power Density**: Relative power consumption per unit area
  + *Critical*: Shows breakdown of Dennard scaling after 28nm
* **Supply Voltage (Vdd)**: Nominal supply voltage
  + *Key trend*: Voltage scaling slowed significantly at advanced nodes
* **SRAM Cell Area**: Area per SRAM bit cell in μm²
  + *Critical insight*: SRAM scaling stalled completely at 5nm

**Practical Application Examples**

**Example 1: SoC Area Estimation**

**Scenario**: You have a 100mm² design on N7, considering N5 migration

**Steps**:

1. Set base node to "7nm" in scaling mode
2. Look at "5nm" transistor density scaling factor: ~1.5x
3. **Interpretation**: Same functionality could fit in ~67mm² on N5
4. **Reality check**: Account for non-scaling components (I/O, analog, SRAM)

**Example 2: Performance vs Cost Trade-off**

**Scenario**: Choosing between N7, N5, and N3 for a new processor

**Steps**:

1. Use absolute values mode
2. Compare transistor density: N7 (91.2) → N5 (137.6) → N3 (220)
3. Note SRAM scaling: N7 (0.031) → N5 (0.021) → N3 (0.021)
4. **Key insight**: N5→N3 gives logic density improvement but no SRAM benefit
5. **Decision factor**: Is the cost premium of N3 justified for your application?

**Example 3: Historical Competitive Analysis**

**Scenario**: Understanding when competitors introduced products

**Steps**:

1. Use table mode with year information
2. Cross-reference with known product launches
3. **Example**: iPhone 12 (2020) used N5, first commercial 5nm product
4. **Insight**: Technology adoption timing affects market positioning

**Critical Insights and Limitations**

**What the Data Shows**

* **Dennard Scaling Breakdown**: Power density increases dramatically after 28nm
* **SRAM Scaling Crisis**: No SRAM improvement from N5 to N3
* **Cost Scaling Failure**: Each new node becomes more expensive per transistor
* **Marketing vs Reality**: Node names (5nm, 3nm) don't reflect physical dimensions

**What to Watch Out For**

**High Density vs High Performance Libraries**

* Tool shows HD (high-density) numbers
* Real CPUs/GPUs use HP (high-performance) libraries
* **Rule of thumb**: Reduce density numbers by ~30% for realistic estimates

**Design-Dependent Scaling**

* Actual area scaling depends on your design composition
* **SRAM-heavy designs**: Get less benefit from new nodes
* **Logic-heavy designs**: See better scaling to advanced nodes

**Non-Scaling Components**

* I/O pads don't scale with technology
* Analog blocks scale poorly
* **Impact**: Large I/O-dominated chips see minimal area reduction

**Integration with EDA Workflow**

**Early Architecture Phase**

* Use scaling factors to set area/power targets
* Validate feasibility of technology choices
* Plan for non-scaling component impact

**Technology Selection**

* Compare multiple node options systematically
* Factor in design complexity and available IP
* Consider cost vs performance trade-offs

**Design Review Gates**

* Reference tool data in architecture reviews
* Validate area estimates against scaling trends
* Document technology selection rationale

**Advanced Usage Tips**

**Custom Analysis**

* Export data for custom analysis in spreadsheets
* Combine with your own cost/yield models
* Cross-reference with foundry roadmaps

**Competitive Intelligence**

* Track competitor technology adoption patterns
* Understand performance/power positioning
* Identify market timing opportunities

**Risk Assessment**

* Evaluate technology migration risks using historical data
* Plan for yield ramp and cost evolution
* Assess supply chain implications

**Data Sources and Reliability**

**Primary Sources:**

* TSMC official specifications and technology symposiums
* WikiChip detailed technical analysis
* Angstronomics reverse-engineering and measurements
* Industry conference papers (IEDM, VLSI Symposium)

**Data Confidence:**

* **High confidence**: N7, N5 data (production proven)
* **Medium confidence**: N3 data (early production)
* **Lower confidence**: N2 projections (roadmap estimates)

**Update Frequency:**

* Tool should be updated as new process data becomes available
* Foundry specifications often evolve during ramp-up
* Consider data vintage when making critical decisions

**Conclusion**

This scaling reference tool provides a foundation for making informed technology decisions in VLSI design. Remember that it's a starting point for analysis - always validate critical assumptions with foundry-specific data for your actual design requirements.

The semiconductor industry's transition to post-Dennard scaling era requires more nuanced decision-making than simple node-to-node migration. Use this tool to understand the broader trends and trade-offs, but always consider your specific application requirements and constraints.